Low Power High Speed Adaptive Vector Equalization: From the Nonlinear Algorithm to a Reconfigurable Analog Circuit

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Abstract:

In this paper we revisit the problem of vector equalization based on continuous-time recurrent neural networks.
We provide simulation results, which verify the accuracy of the analog circuit as a representation of the continuous-time recurrent neural network, at the same time emphasizing the remarkable properties of the analog solution, in terms of computational speed and dissipated power. We place emphasis on the minimization of the equalization time, of the equivalent time constant, without foregoing the flexibility to adapt the circuit in run-time to all possible channels. As a case st udy, a 4- neurons fully-adaptive equalizer in IHP 0.25 µm SiGe BiCMOS technology is presented, for BPSK modulation scheme, which can achieve a throughput up to 19.5 Gbps, with a static power dissipation of 35 mW. This corresponds to an increase of the power-to-speed ratio of up to four orders of magnitude compared to a standard digital solution.